Amendments to the Claims:

This following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) An electronic automation system comprising:

a ~~shape-based~~ database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the ~~shape-based~~ database, based on input from the mouse input device; and

[[an]] a shape-based automatic router tool, capable of accessing the ~~shape-based~~ database, using flood operations to create [[a]] an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths.

2. (currently amended) The system of claim 1 further comprising:

a file, accessible by the automatic router tool, comprising a current density table comprising current density as a function of at least one of layer, net frequency, or track width~~, accessible by the automatic router tool~~.

3. (original) The system of claim 1 further comprising:

a file, accessible by the automatic router tool, comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, DC operation of the net will be assumed.

4. (original) The system of claim 1 further comprising:

a file, accessible by the automatic router tool, comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, a warning message is presented.

5. (currently amended) The system of claim 1 wherein the automatic router tool uses at least one of Steiner tree algorithm, heuristic Steiner tree creation algorithm, or batched greedy algorithm ~~Batched Greedy Algorithm~~.

6. (canceled)

7. (original) The system of claim 1 wherein the integrated circuit design comprises at least one of a memory integrated circuit, DRAM, EPROM, EEPROM, Flash memory, ASIC, microprocessor, programmable logic device, field programmable gate array, digital signal processor, analog integrated circuit, amplifier circuit, system on a chip, or programmable system-on-a-chip.

8. (original) The system of claim 1 wherein automatic router tools creates interconnect route paths for two or more nets, and the interconnect route paths are for one layer of the integrated circuit design.

9. (currently amended) A method of designing an integrated circuit comprising:

using at least one flooding operation to determine ~~determining~~ an interconnect route path between a first point and a second point of an integrated circuit design;

comparing a property of the interconnect route path to a design rule;

if the property of the first interconnect path violates the design rule, creating an interconnect line for the interconnect route path having a first width; and

if the property of the first interconnect path meets the design rule, creating the interconnect line for the interconnect route path having a second width, different from the first width.

10. (original) The method of claim 9 wherein the property is a current requirement of the interconnect route path.

11. (original) The method of claim 9 wherein the design rule is a current density rule.

12. (original) The method of claim 9 wherein the design rule is an optical proximity effect correction rule.

13. (currently amended) A method of designing an integrated circuit comprising:

using at least one flooding operation to determine ~~determining~~ an interconnect route path between a first point and a second point of an integrated circuit design;

determining a property of the interconnect route path; and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and a design rule.

14. (original) The method of claim 13 wherein the design rule addresses at least one of current density, optical proximity effects, current handling, power handling, reliability, electromigration, voltage drop, or self-heating.

15–20. (canceled)

21. (new) The system of claim 1 wherein automatic router tools creates interconnect route paths for a first net, a second net, and a third net, each of the first, second, and third nets carrying different signals, and

the first net comprises segments having different interconnect widths, the signal net comprises segments having different interconnect widths, and the third net comprises segments having different interconnect widths.

22. (new) The system of claim 1 wherein the automatic router tool performs detailed routing.

23. (new) An electronic design automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device; and

an automatic shape-based router tool, capable of accessing the database, using a batched greedy algorithm to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths.

24. (new) An electronic automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device;

a shape-based automatic router tool, capable of accessing the shape-based database, to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths; and

a file, accessible by the shape-based automatic router tool, comprising a current density table comprising current density as a function of net frequency.

25. (new) An electronic automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device;

a shape-based automatic router tool, capable of accessing the shape-based database, to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths; and

a file, accessible by the shape-based automatic router tool, comprising frequency information for one or more nets of integrated circuit.

26. (new) The system of claim 25 wherein when frequency information is not provided for a net, DC operation of the net will be assumed.

27. (new) The system of claim 25 wherein when frequency information is not provided for a net, a warning message is presented.

28. (new) The system of claim 24 wherein the shape-based automatic router tool uses a batched greedy algorithm to create the interconnect route path.

29. (new) The system of claim 25 wherein the shape-based automatic router tool uses a batched greedy algorithm to create the interconnect route path.

30. (new) A method of designing an integrated circuit comprising:

automatically determining an interconnect route path between a first point and a second point of an integrated circuit design;

determining a property of the interconnect route path; and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and optical proximity effects.